

FEATURES

- 4 A peak current ($<2 \Omega R_{DS(on)}$)
- 2.5 V to 6.5 V input supply voltage
- 4.5 V to 35 V output supply voltage
- UVLO V_{DD1} positive going threshold: 2.5 V maximum
- Multiple UVLO options for V_{DDA} and V_{DDB} positive going threshold
 - Grade A: 4.5 V maximum
 - Grade B: 7.5 V maximum
 - Grade C: 11.6 V maximum
- Precise timing characteristics
 - 44 ns maximum propagation delay
- Adjustable dead time and dual input (ADuM4221)
- Adjustable dead time and single input (ADuM4221-1)
- CMOS input logic levels
- High common-mode transient immunity: 150 kV/ μ s
- High junction temperature operation: 125°C
- Default low output
- Safety and regulatory approvals (pending)
 - UL recognition per UL 1577
 - 5700 V rms for 1 minute duration
 - CSA Component Acceptance Notice 5A
 - VDE certificate of conformity
 - DIN V VDE V 0884-11: $V_{IORM} = 849$ V peak
- Increased creepage wide body, 16-lead SOIC_IC

APPLICATIONS

- Switching power supplies
- Isolated IGBT/MOSFET gate drives
- Industrial inverters
- Gallium nitride (GaN)/silicon carbide (SiC) compatible

GENERAL DESCRIPTION

The ADuM4221/ADuM4221-1 are 4 A isolated, half bridge gate drivers that employ the Analog Devices, Inc., iCoupler® technology to provide independent and isolated high-side and low-side outputs. The ADuM4221/ADuM4221-1 provide 5700 V rms isolation in an [increased creepage wide body, 16-lead SOIC_IC](#). Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The isolators operate with a logic input voltage ranging from 2.5 V to 6.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers employing high voltage level translation methodologies, the ADuM4221/ADuM4221-1 offer the benefit of true, galvanic isolation between the input and each output.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

Rev. A

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FUNCTIONAL BLOCK DIAGRAMS

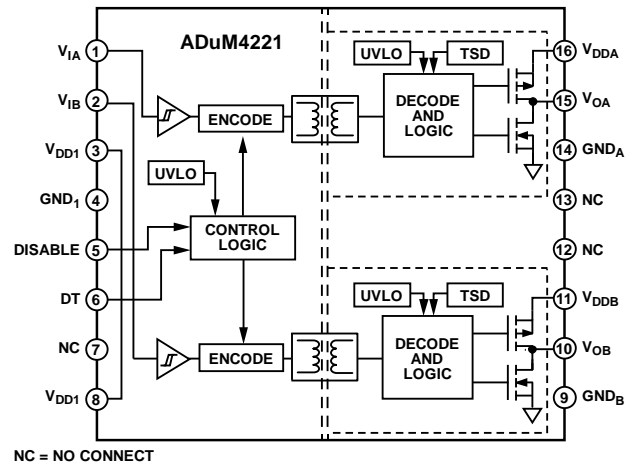


Figure 1. ADuM4221

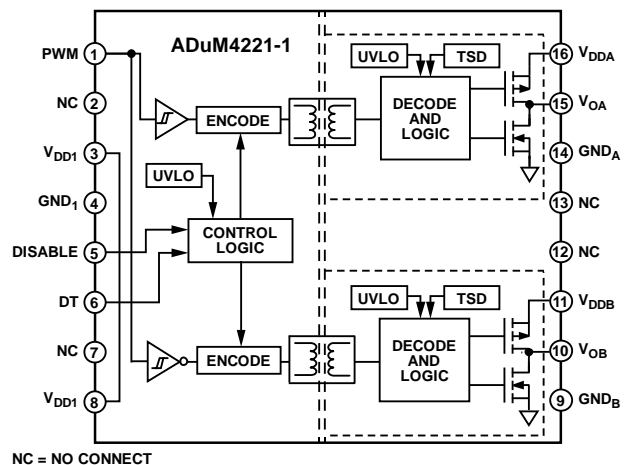


Figure 2. ADuM4221-1

The ADuM4221/ADuM4221-1 each have built in overlap protection and allow dead time adjustment. A single resistor between the dead time pin (DT) and the GND₁ pin sets the dead time on the secondary side between the high-side and the low-side outputs.

An internal thermal shutdown (TSD) sets outputs low if the internal temperature on the ADuM4221/ADuM4221-1 exceeds the TSD temperature. As a result, the ADuM4221/ADuM4221-1 provide reliable control over the switching characteristics of the insulated gate bipolar transistor (IGBT)/metal-oxide semiconductor field effect transistor (MOSFET) configurations over a wide range of positive or negative switching voltages.

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REVISION HISTORY

8/2020—Rev. 0 to Rev. A

Add ADuM4221-1.....	Universal
Added Figure 2; Renumbered Sequentially	1
Changes to Input Supply Current, Quiescent Parameter,	
Table 1	3
Changes to Table 7	7
Changes to Figure 4 Caption, Table 10 Caption, and Table 11	
Caption	8
Add Figure 5, Table 12, and Table 13; Renumbered Sequentially...	9
Added Figure 10	10
Changes to Figure 8 Caption, Figure 9 Caption, and Figure 11	
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Changes to Figure 12 Captions.....	11
Changes to Figure 28 and TSD Section.....	15
Changes to Figure 30 and Adjustable Dead Time Control	
Section	16
Added Figure 33.....	17
Changes to Bootstrapped, Half Bridge Operation Section and	
Figure 34 Caption.....	18

7/2020—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to GND_I, high-side voltages referenced to GND_A, GND_B, $2.5\text{ V} \leq V_{DD1} \leq 6.5\text{ V}$, $4.5\text{ V} \leq V_{DDA}, V_{DDB} \leq 35\text{ V}$, and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_J = 25^\circ\text{C}$, $V_{DD1} = 5.0\text{ V}$, and V_{DDA} and $V_{DDB} = 15\text{ V}$.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic Input Voltage	V_{DD1}	2.5		6.5	V	
Output Supply Voltage	V_{DDA}, V_{DDB}	4.5		35	V	
Input Supply Current, Quiescent	$I_{DD1(Q)}$					
Input A High/PWM High or Input B High			7.2	10	mA	
Both Inputs Low (ADuM4221 Only)			1.4	2.4	mA	
Output Supply Current, Per Channel, Quiescent	$I_{DD2(Q)}$					
Output Channel						
High			1.4	2.6	mA	
Low			1.6	2.1	mA	
Input Currents	I_{IA}, I_{IB}	-1	+0.01	+1	μA	
Input Voltage						
Input Threshold						
Logic High	V_{IH}	$0.7 \times V_{DD1}$			V	$2.5\text{ V} \leq V_{DD1} \leq 5\text{ V}$
		3.5			V	$V_{DD1} > 5\text{ V}$
Logic Low	V_{IL}			$0.3 \times V_{DD1}$	V	$2.5\text{ V} \leq V_{DD1} \leq 5\text{ V}$
				1.5	V	$V_{DD1} > 5\text{ V}$
Undervoltage Lockout (UVLO)						
V_{DD1} Positive Going Threshold	$V_{VDD1UV+}$		2.45	2.5	V	
V_{DD1} Negative Going Threshold	$V_{VDD1UV-}$	2.3	2.35		V	
V_{DD1} Hysteresis	$V_{VDD1UVH}$		0.1		V	
V_{DDA} and V_{DDB} Positive Going Threshold	$V_{VDDAUV+},$ $V_{VDDBUV+}$		4.4	4.5	V	Grade A
			7.3	7.5	V	Grade B
			11.3	11.6	V	Grade C
V_{DDA} and V_{DDB} Negative Going Threshold	$V_{VDDAUV-},$ $V_{VDDBUV-}$	4.1	4.2		V	Grade A
		6.9	7.1		V	Grade B
		10.8	11.1		V	Grade C
V_{DDA} and V_{DDB} Hysteresis	$V_{VDDAUVH},$ $V_{VDDBUVH}$		0.2		V	Grade A
			0.2		V	Grade B
			0.2		V	Grade C
TSD						
Positive Edge	T_{TSD_POS}		155		$^\circ\text{C}$	
Hysteresis	T_{TSD_HYST}		30		$^\circ\text{C}$	
Drive Strength						
Pull-Down N Channel Metal Oxide Semiconductor (NMOS) On Resistance	$R_{DS(on)_N}$		0.6	1.6	Ω	Tested at 250 mA, $V_{DDx} = 15\text{ V}$
			0.6	1.6	Ω	Tested at 1 A, $V_{DDx} = 15\text{ V}$
Pull-Up P Channel Metal Oxide Semiconductor (PMOS) On Resistance	$R_{DS(on)_P}$		0.8	1.8	Ω	Tested at 250 mA, $V_{DDx} = 15\text{ V}$
			0.8	1.8	Ω	Tested at 1 A, $V_{DDx} = 15\text{ V}$
Peak Current	I_{PEAK}		4		A	$V_{DDA}, V_{DDB} = 15\text{ V}, 2\ \Omega$ gate resistance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
Pulse Width		50			ns	Load capacitance (C_L) = 2.2 nF, $V_{DD1} = 5$ V, V_{DDA} and $V_{ddb} = 15$ V, external gate resistor (R_G) = 5.1 Ω
Propagation Delay ¹						$C_L = 2.2$ nF, $V_{DD1} = 5$ V, V_{DDA} and $V_{ddb} = 15$ V, and $R_G = 5.1$ Ω
Rising Edge	t_{DLH}	19	25	33	ns	
Falling Edge	t_{DHL}	21	30	44	ns	
Time to Disable	t_{DIS}	21	25	44	ns	
Time to Enable	t_{EN}	19	25	33	ns	
Delay Skew ²	t_{PSK}			22	ns	$C_L = 2.2$ nF, $R_G = 5.1$ Ω
Pulse Width Distortion	t_{PWD}		5	16	ns	$C_L = 2.2$ nF, $V_{DD1} = 5$ V, V_{DDA} and $V_{ddb} = 15$ V, $R_G = 5.1$ Ω
Channel to Channel Matching ³	t_{PSKCD}		1.5	10	ns	$C_L = 2.2$ nF, $V_{DD1} = 5$ V, V_{DDA} and $V_{ddb} = 15$ V, see Figure 22
Output Rise and Fall Time (10% to 90%)	t_R/t_F	14	25	34	ns	$C_L = 2.2$ nF, $V_{DD1} = 5$ V, V_{DDA} and $V_{ddb} = 15$ V, $R_G = 5.1$ Ω , see Figure 29
Adjustable Dead Time	DT					$C_L = 2.2$ nF, $V_{DD1} = 5$ V, V_{DDA} and $V_{ddb} = 15$ V, $R_G = 5.1$ Ω
		1809	2320	2831	ns	Dead time resistor (R_{DT}) = 500 k Ω
		742	938	1135	ns	$R_{DT} = 200$ k Ω
		48	62	76	ns	$R_{DT} = 10$ k Ω

¹ t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH} , to the output rising 10% level of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL} , to the output falling 90% threshold of the V_{Ox} signal. See Figure 29 for the waveforms of the propagation delay parameters.

² t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 29 for the waveforms of the propagation delay parameters.

³ Channel to channel matching is the absolute value of the difference in propagation delays between two channels on a single device.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) ¹	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output) ¹	C_{I-O}		2.2		pF	$f = 1$ MHz
Input Capacitance ²	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		$^{\circ}\text{C}/\text{W}$	Thermocouple located at center of package underside

¹ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM4221/ADuM4221-1 is pending approval by the organizations listed in Table 3.

Table 3.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized Under 1577 Component Recognition Program ¹ Single Protection, 5700 V rms Isolation Voltage File E214100	Approved under CSA Component Acceptance Notice 5A IEC 62368, Third Edition Basic insulation at 830 V rms (1173 V peak) Reinforced insulation at 415 V rms (586 V peak) IEC 60601-1, Edition 3.1 Reinforced insulation (2 MOPP), 250 V rms (353V peak) CSA 61010-1-12 and IEC 61010-1, Third Edition Basic insulation at 300 V rms mains, 800 V secondary (1089 V peak) Reinforced insulation at 300 V rms mains, 400 V secondary (565 V peak) File 205078	Certified according to DIN VDE V 0884-11 (VDE V 0884-11):2017-01 ² Basic insulation, 900 V peak, V _{IOSM} = 9850 V peak Reinforced insulation, 849 V peak, V _{IOSM} = 8000 V peak File 2471900-4880-0003	Certified by CQC11-471543-2012 GB4943.1-2011 Basic insulation at 800 V rms (1131 V peak) Reinforced insulation at 400 V rms (565 V peak) File (pending)

¹ In accordance with UL 1577, each ADuM4221/ADuM4221-1 is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec.

² In accordance with DIN VDE V 0884-11, each ADuM4221/ADuM4221-1 is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN VDE V 0884-11 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS**Table 4.**

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board, PCB (PCB Clearance)	L (PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	μ m	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Protective circuits ensure maintenance of the safety data.

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 600 V rms			I to IV I to IV I to IV	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Peak Isolation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1019	V peak
Maximum Rated Transient Isolation Voltage		V_{IOTM}	8000	V peak
Surge Isolation Voltage		V_{IOSM}		
Basic	V peak = 12.8 kV, 1.2 μs rise time, 50 μs, 50% fall time		9850	V peak
Reinforced	V peak = 12.8 kV, 1.2 μs rise time, 50 μs, 50% fall time		8000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_s	150	°C
Total Power Dissipation at 25°C		P_s	2.77	W
Insulation Resistance at T_s	$V_{IO} = 500$ V	R_s	>10 ⁹	Ω

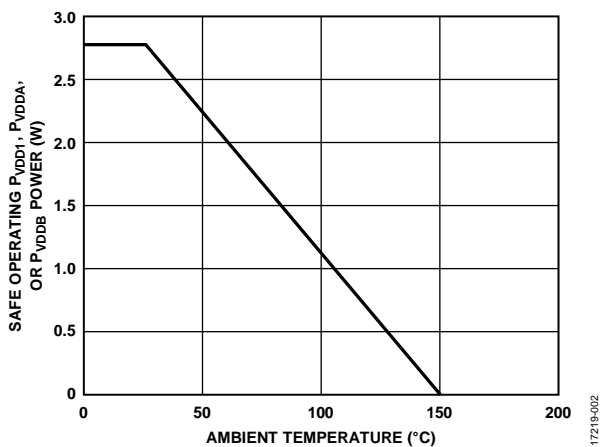


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-11

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
T_J	-40°C to +125°C
Supply Voltages	
V_{DD1} ¹	2.5 V to 6.5 V
V_{DDA} and V_{DDB} ²	4.5 V to 35 V
Common-Mode Transient Immunity	
Static ³	-150 kV/μs to +150 kV/μs
Dynamic ⁴	-150 kV/μs to +150 kV/μs
Dead Time Resistor Range	10 kΩ to 500 kΩ

¹ Referenced to GND₁.

² Referenced to GND_A and GND_B.

³ Static common-mode transient immunity is defined as the largest dv/dt between GND₁ and GND_A and GND_B with the inputs held either high or low such that the output voltage remains either above 0.8 × V_{DDA} and V_{DDB} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.

⁴ Dynamic common-mode transient immunity is defined as the largest dv/dt between GND₁ and GND_A and GND_B with the switching edge coincident with the transient test pulse. Operation with transients above recommended levels can cause momentary data upsets.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
Voltage Ranges	
Supply	
V_{DD1}	-0.2 V to +7 V
V_{DDA} and V_{DDB}	-0.3 V to +40 V
Input ¹ (V_{IA} , V_{IB} , PWM, and DISABLE)	-0.3 V to +7 V
Output ²	
V_{OA}	-0.3 V to $V_{DDA} + 0.3$ V
V_{OB}	-0.3 V to $V_{DDB} + 0.3$ V
V_{OA} Transient for 200 ns	-2 V to $V_{DDA} + 0.3$ V
V_{OB} Transient for 200 ns	-2 V to $V_{DDB} + 0.3$ V
Temperature Range	
Storage (T_{ST})	-55°C to +150°C
T_J	-40°C to +125°C
Common-Mode Transients ³ (CM_H , CM_L)	-200 kV/ μs to +200 kV/ μs

¹ Rating assumes V_{DD1} is above 2.5 V. V_{IA} , V_{IB} , and PWM are rated up to 6.5 V when V_{DD1} is unpowered.

² Referenced to GND_2 , maximum of 40 V.

³ Refers to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and Ψ_{JT} is the junction to top characterization parameter.

Table 8. Thermal Resistance

Package Type ¹	θ_{JA}	Ψ_{JT}	Unit
RI-16-2	45	16.67	°C/W

¹ 4-layer PCB.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage¹

Parameter	Rating	Unit	Constraint
AC Voltage			
Bipolar Waveform			
Basic Insulation	900	V peak	20 year minimum insulation lifetime per VDE-0884-11
Reinforced Insulation	849	V peak	20 year minimum insulation lifetime per VDE-0884-11
DC Voltage			
Basic Insulation	1660	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60664-1, Pollution Degree 2, Material Group I
Reinforced Insulation	830	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60664-1, Pollution Degree 2, Material Group I

¹ Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

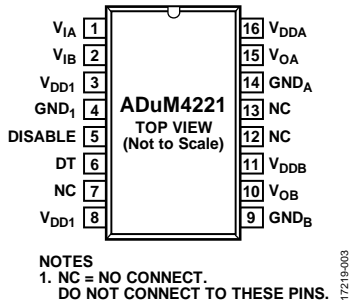


Figure 4. ADuM4221 Pin Configuration

Table 10. ADuM4221 Pin Function Descriptions

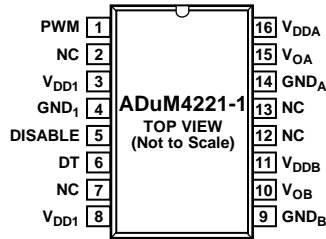
Pin No. ¹	Mnemonic	Description
1	V _{IA}	Logic Input A.
2	V _{IB}	Logic Input B.
3, 8	V _{DD1}	Input Supply Voltage.
4	GND ₁	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. The DISABLE pin disables the isolator inputs and refresh circuits.
6	DT	Dead Time Control Input. The resistor connected from the DT pin to ground sets the dead time between the output transitions.
7, 12, 13	NC	No Connect. Do not connect to these pins.
9	GND _B	Ground Reference for Output B.
10	V _{OB}	Output B.
11	V _{DDB}	Output B Supply Voltage.
14	GND _A	Ground Reference for Output A.
15	V _{OA}	Output A.
16	V _{DDA}	Output A Supply Voltage.

¹ Pin 3 and Pin 8 are internally connected. Connecting both the V_{DD1} pins to the V_{DD1} input supply is recommended.

Table 11. ADuM4221 Truth Table (Positive Logic with Dead Time)

DISABLE ¹	V _{IA} Input ¹	V _{IB} Input ¹	V _{DD1} State	V _{DDA} and V _{DDB} State	V _{OA} Output	V _{OB} Output	Notes
Low	Low	Low	Powered	Powered	Low	Low	Output transition begins after dead time expires
Low	Low	High	Powered	Powered	Low	High	Output transition begins after dead time expires
Low	High	Low	Powered	Powered	High	Low	Output transition begins after dead time expires
Low	High	High	Powered	Powered	Low	Low	Output transition begins after dead time expires
High	X	X	Powered	Powered	Low	Low	Device is disabled
X	X	X	Unpowered	Powered	Low	Low	Output returns to input state after V _{DD1} power restoration
X	X	X	Powered	Unpowered	Low	Low	Output remains low

¹ X means don't care.



NOTES
 1. NC = NO CONNECT.
 DO NOT CONNECT TO THESE PINS.

17219-303

Figure 5. ADuM4221-1 Pin Configuration

Table 12. ADuM4221-1 Pin Function Descriptions

Pin No. ¹	Mnemonic	Description
1	PWM	Logic Input.
2, 7, 12, 13	NC	No Connect. Do not connect to these pins.
3, 8	V _{DD1}	Input Supply Voltage.
4	GND ₁	Ground Reference for Input Logic Signals.
5	DISABLE	Input Disable. Disables the isolator inputs and refresh circuits.
6	DT	Dead Time Control Input. The resistor connected from the DT pin to ground sets the dead time between the output transitions.
9	GND _B	Ground Reference for Output B.
10	V _{OB}	Inverting Output B.
11	V _{DDB}	Output B Supply Voltage.
14	GND _A	Ground Reference for Output A.
15	V _{OA}	Noninverting Output A.
16	V _{DDA}	Output A Supply Voltage.

¹ Pin 3 and Pin 8 are internally connected. Connecting both the V_{DD1} pins to the V_{DD1} input supply is recommended.

Table 13. ADuM4221-1 Truth Table (PWM Input with Dead Time)

DISABLE ¹	PWM Input ¹	V _{DD1} State	V _{DDA} and V _{DDB} State	V _{OA} Output	V _{OB} Output	Notes
Low	Low	Powered	Powered	Low	High	Output transition begins after dead time expires
Low	High	Powered	Powered	High	Low	Output transition begins after dead time expires
High	X	Powered	Powered	Low	Low	Device is disabled
X	X	Unpowered	Powered	Low	Low	Output returns to an input state after V _{DD1} power restoration
X	X	Powered	Unpowered	Low	Low	Output remains low

¹ X means don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

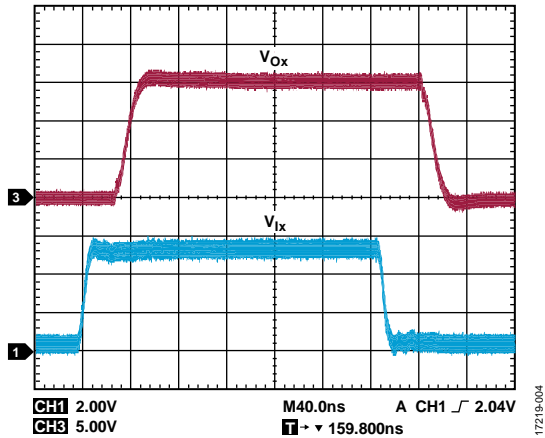


Figure 6. Output Waveform for 2 nF Load and 3.9 Ω Series Gate Resistor with 15 V Output Supply

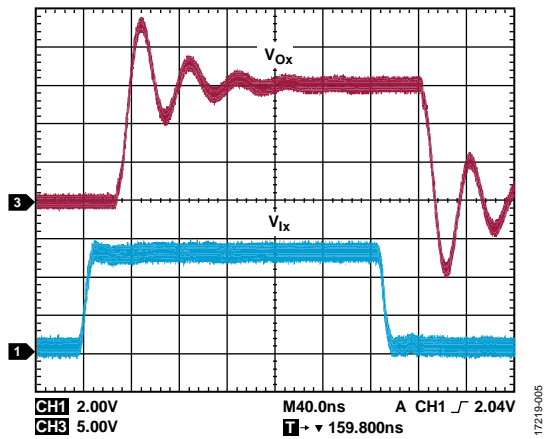


Figure 7. Output Waveform for 2 nF Load and 0 Ω Series Gate Resistor with 15 V Output Supply

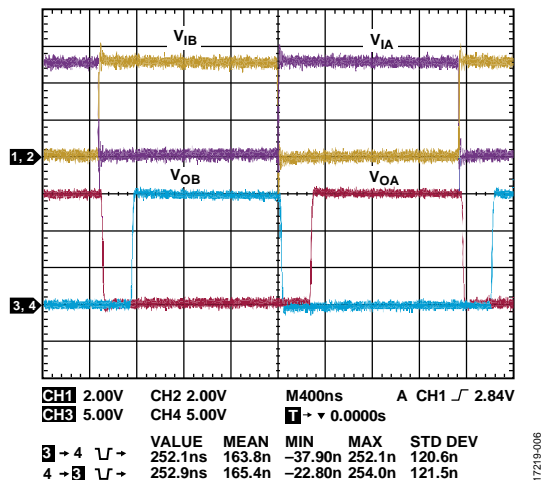


Figure 8. Dead Time Operation Between Input and Output with 50 kΩ Dead Time Resistor (ADuM4221 Only)

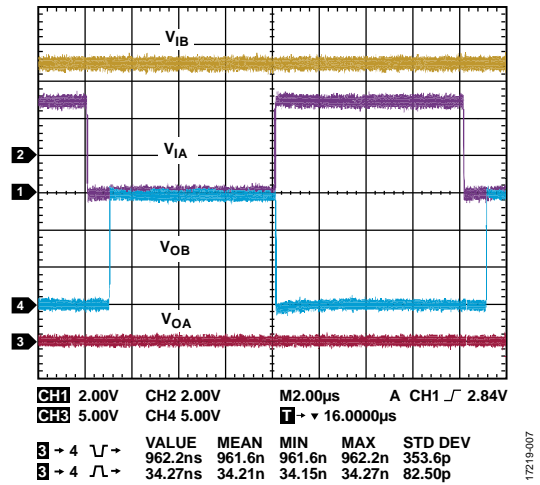


Figure 9. Dead Time Operation Between Input and Output with 200 kΩ Dead Time Resistor and One Input Held High (ADuM4221 Only)

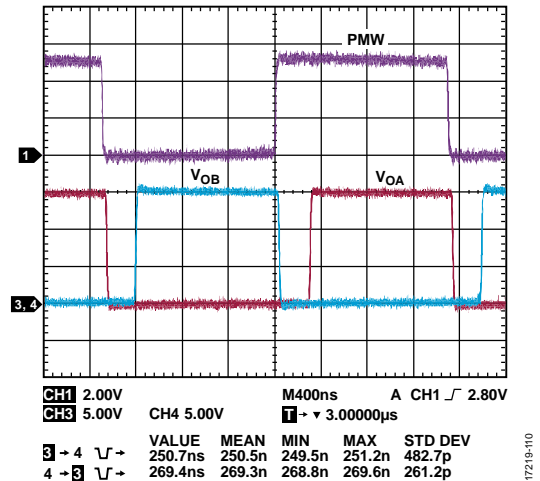


Figure 10. Dead Time Operation Between Input and Output with 50 kΩ Dead Time Resistor (ADuM4221-1 Only)

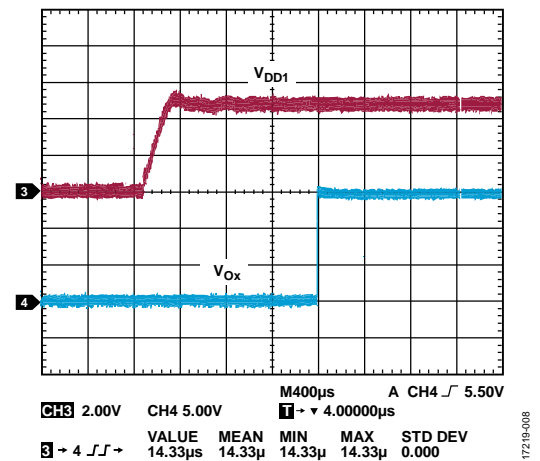


Figure 11. Typical V_{DD1} Delay to Output Waveform, $V_{Ix} = V_{DD1}$ and $PWM = V_{DD1}$ or GND_1

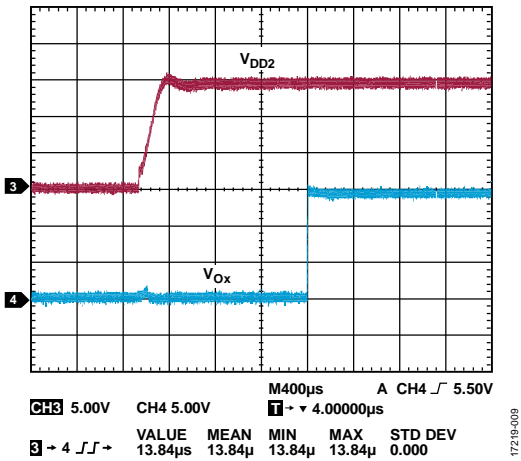


Figure 12. Typical V_{DD2} Delay to Output Waveform, $V_{ik} = V_{DD1}$ and $PWM = V_{DD1}$ or GND_1 (V_{DD2} Refers to V_{DDA} or V_{DDB})

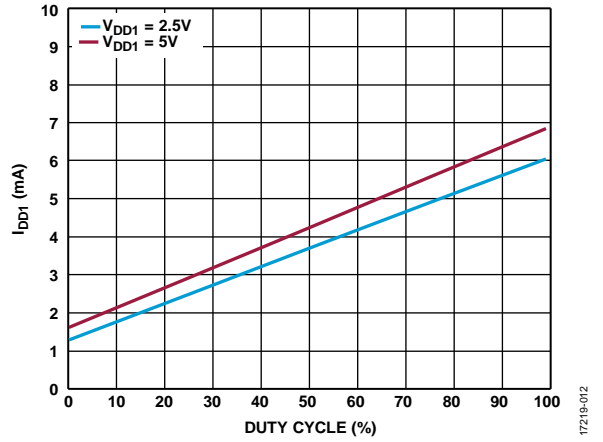


Figure 15. I_{DD1} vs. Duty Cycle for $V_{DD1} = 2.5V$ and $V_{DD1} = 5V$, $V_{DD2} = 15V$ (V_{DD2} Refers to V_{DDA} or V_{DDB})

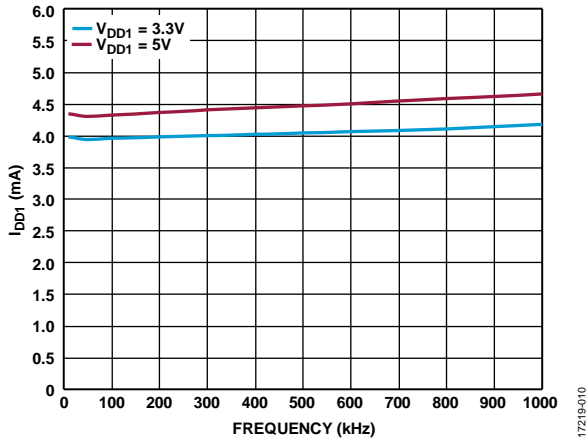


Figure 13. V_{DD1} Current (I_{DD1}) vs. Frequency for $V_{DD1} = 3.3V$ and $V_{DD1} = 5V$, 50% Duty Cycle

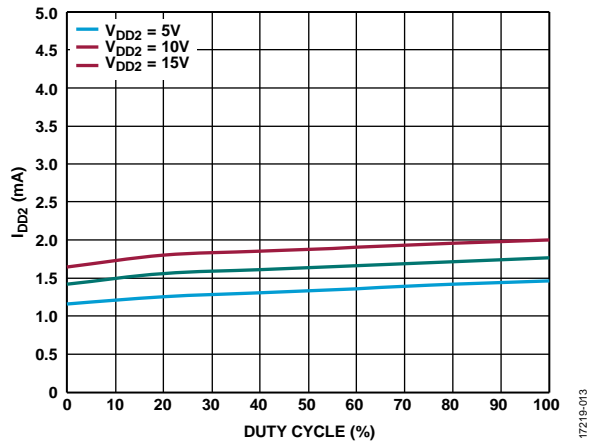


Figure 16. I_{DD2} vs. Duty Cycle for $V_{DD2} = 5V$, $V_{DD2} = 10V$, and $V_{DD2} = 15V$, $V_{DD1} = 5V$ (V_{DD2} Refers to V_{DDA} or V_{DDB})

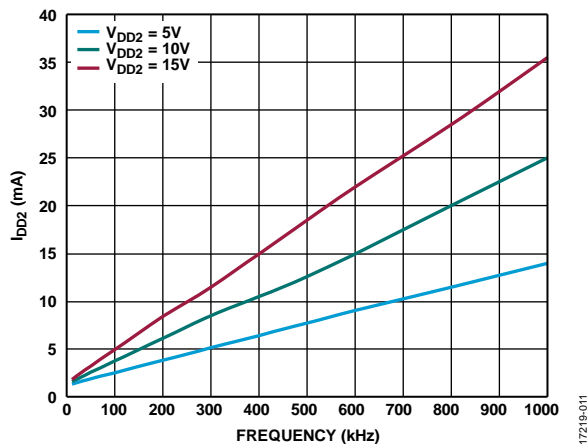


Figure 14. V_{DD2} Current (I_{DD2}) vs. Frequency for $V_{DD2} = 5V$, $V_{DD2} = 10V$, and $V_{DD2} = 15V$, 50% Duty Cycle, 2 nF Load (V_{DD2} Refers to V_{DDA} or V_{DDB})

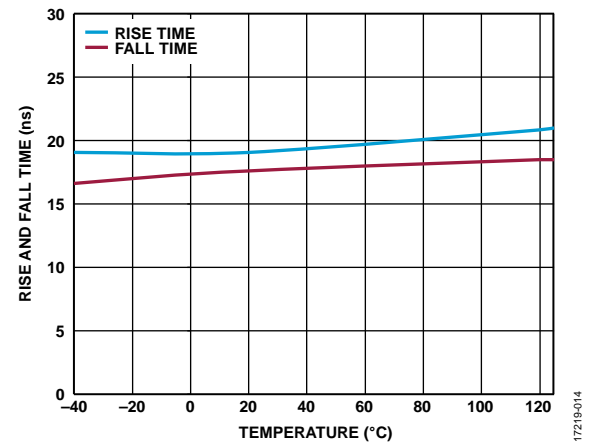


Figure 17. Rise and Fall Time vs. Temperature with a 3.9Ω Series Gate Resistor for a 2 nF Load and a 15 V Output Supply

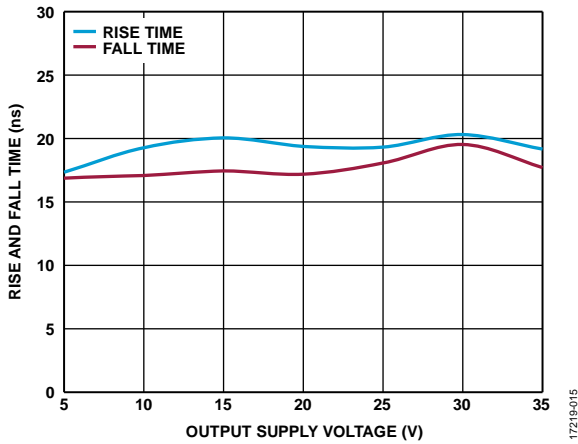


Figure 18. Rise and Fall Time vs. Output Supply Voltage with a 3.9 Ω Series Gate Resistor for a 2 nF Load

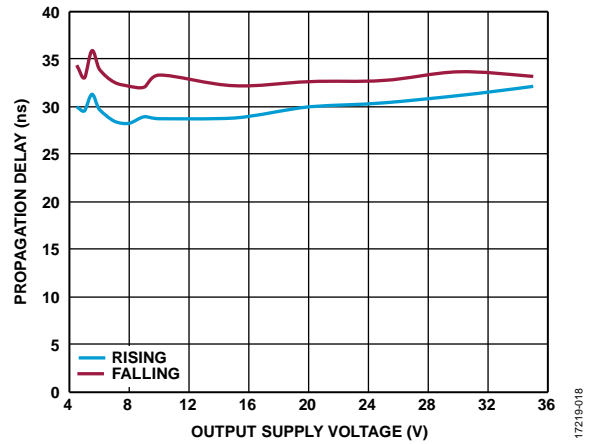


Figure 21. Propagation Delay vs. Output Supply Voltage, Rising and Falling, $V_{DD1} = 5\text{ V}$

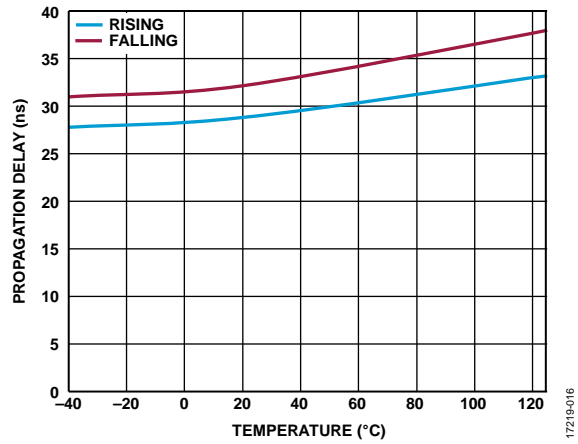


Figure 19. Propagation Delay vs. Temperature

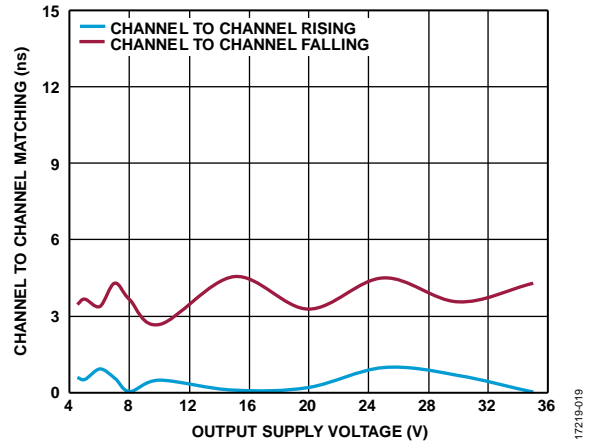


Figure 22. Channel to Channel Matching vs. Output Supply Voltage, Rising and Falling

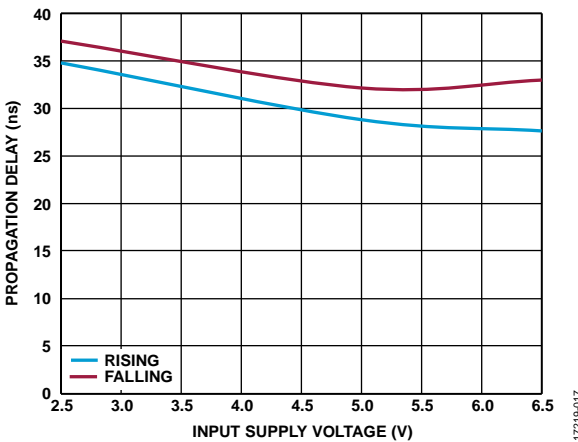


Figure 20. Propagation Delay vs. Input Supply Voltage, Rising and Falling, $V_{DD2} = 15\text{ V}$ (V_{DD2} Refers to V_{DDA} or V_{ddb})

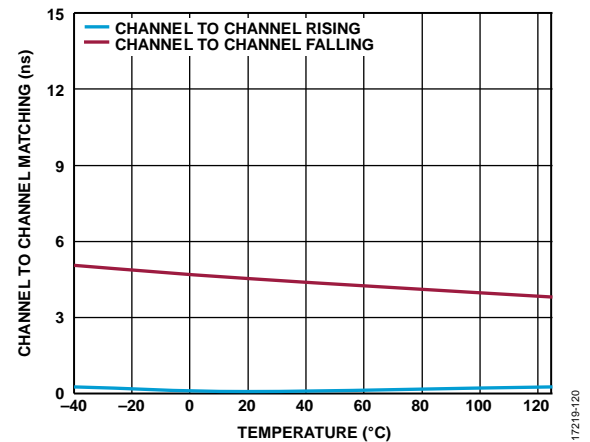


Figure 23. Channel to Channel Matching vs. Temperature, Rising and Falling, $V_{DD2} = 15\text{ V}$ (V_{DD2} Refers to V_{DDA} or V_{ddb})

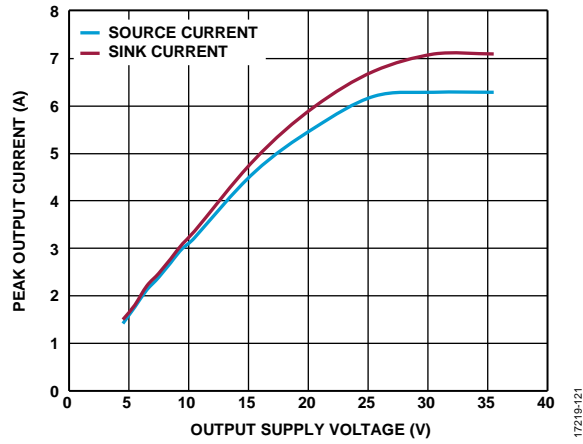


Figure 24. Peak Output Current vs. Output Supply Voltage with a 2.2 Ω Series Gain Resistor

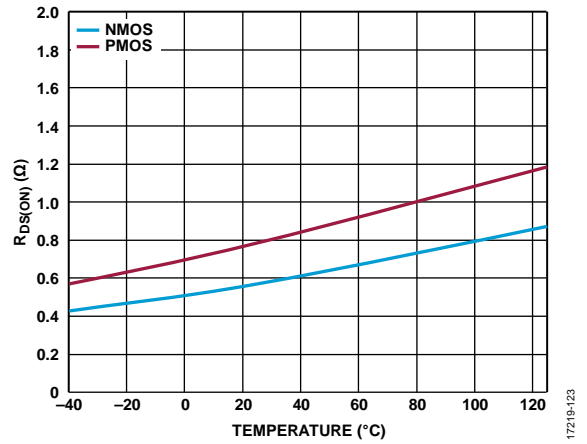


Figure 26. $R_{DS(ON)}$ vs. Temperature for NMOS and PMOS

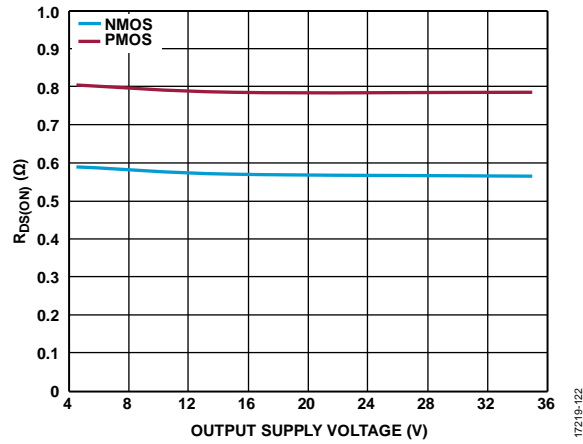


Figure 25. Output Resistance ($R_{DS(ON)}$) vs. Output Supply Voltage for NMOS and PMOS, $V_{DD1} = 5 V$

THEORY OF OPERATION

Gate drivers are required where fast rise times of switching device gates are desired. The gate signal for most enhancement type power devices is referred to a source or emitter node. The gate driver must have the ability to follow this source or emitter node, necessitating isolation between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of the drive strength of the gate driver. Buffer stages before a CMOS output reduce the total delay time and increase the final drive strength of the driver.

The ADuM4221/ADuM4221-1 each achieve isolation between the control side and output side of the gate driver by means of a high frequency carrier that transmits data across the isolation barrier using *iCoupler* chip scale transformer coils separated by

layers of polyimide isolation. The encoding scheme used by the ADuM4221/ADuM4221-1 is a positive logic on/off keying (OOK), a high signal transmitted by the presence of the carrier frequency across the *iCoupler* chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices, driving in situations where shoot through conditions can exist. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques such as differential coil layout. Figure 27 illustrates the OOK encoding used by the ADuM4221/ADuM4221-1.

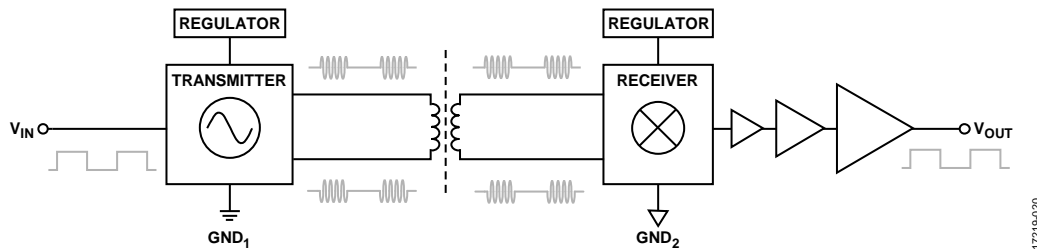


Figure 27. Operational Block Diagram of OOK Encoding (V_{IN} Is the Input Voltage, and V_{OUT} Is the Output Voltage.)

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM4221/ADuM4221-1 require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 28). Use a small ceramic capacitor with a value between 0.01 μF and 0.1 μF to provide a good high frequency bypass. On the output power supply pin, V_{DDA} or V_{DDB} , it is also recommended to add a 10 μF capacitor to provide the charge required to drive the gate capacitance at the ADuM4221/ADuM4221-1 outputs. On the output supply pin, avoid the use of vias with a bypass capacitor or use multiple vias to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must be as short as possible.

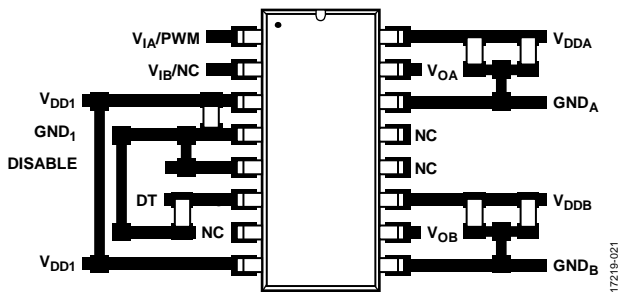


Figure 28. ADuM4221/ADuM4221-1 Recommended PCB Layout

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay parameter describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM4221/ADuM4221-1 specify the rising edge propagation delay (t_{DLH}) as the time between the rising input high logic threshold (V_{IH}) to the output rising (t_{R}) 10% threshold (see Figure 29). Likewise, the falling edge propagation delay (t_{DHL}) is the time between the input falling logic low threshold (V_{IL}) and the output falling (t_{F}) 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, which is the industry standard for gate drivers.

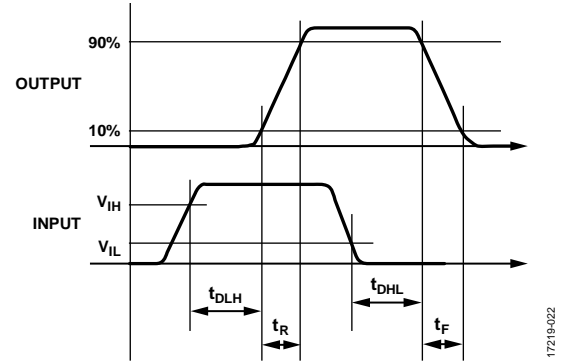


Figure 29. Propagation Delay Parameters

Channel to channel matching is the maximum amount that the propagation delay differs between channels within a single component.

Propagation delay skew is the maximum amount that the propagation delay differs between multiple components operating under the same conditions.

PEAK CURRENT RATING

The ADuM4221/ADuM4221-1 each have two output channels, and each channel connects to the gate of the power device through an external series gate resistor. The output driver MOSFETs of the gate driver IC can source or sink more than 6 A (per V_{OA} and V_{OB}). In a practical application, to control the drive strength and to spread the power dissipation of driving the gate to outside of the gate driver IC, standard external series gate resistors are used. The output current of the gate driver is shown in Figure 24 of the Typical Performance Characteristics section.

PROTECTION FEATURES

TSD

If the internal temperature of the ADuM4221/ADuM4221-1 exceeds 155°C (typical), these devices enter TSD. During the TSD time, the gate drive is disabled and the outputs, V_{OA} and V_{OB} , are driven low. When TSD occurs, the devices do not leave TSD until the internal temperature drops below 125°C (typical), at which time, the devices exit shutdown.

UVLO

The ADuM4221/ADuM4221-1 each have UVLO protections for both the primary and secondary side of the devices. If either the primary or secondary side voltages are below the falling edge UVLO, the devices output a low signal. After the ADuM4221/ADuM4221-1 are powered above the rising edge UVLO threshold, the devices output the signal found at the input. To account for small voltage source ripple, hysteresis is built into the UVLO. The primary side UVLO thresholds are common among all models.

OUTPUT LOAD CHARACTERISTICS

The output signals depend on the characteristics of the output load, which is typically an N channel MOSFET. The driver output response to an N channel MOSFET load with a gate voltage (V_{GATE}) can be modeled with a switch output resistance (R_{SW}), an inductance due to the PCB trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 30.

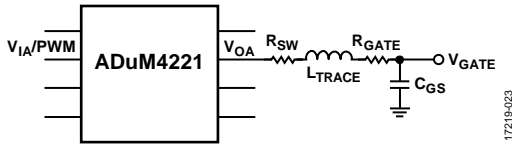


Figure 30. Resistor, Inductor, and Capacitor (RLC) Model of the Gate of an N Channel MOSFET

R_{SW} is the switch resistance of the internal driver output, which is approximately $2\ \Omega$. R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of approximately $1\ \Omega$ and a C_{GS} of between 2 nF and 10 nF. L_{TRACE} is the inductance of the PCB trace, typically a value of 5 nH or less for a well designed layout with a short and wide connection from the ADuM4221/ADuM4221-1 output to the gate of the MOSFET. The following equation defines the Q factor of the RLC circuit, which indicates how the output responds to a step change. For a well damped output, Q is less than 1.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

Output ringing is reduced by adding a series gate resistance to dampen the response. The waveforms in Figure 6 show a correctly damped example with a 2 nF load and a 3.9 Ω external series gate resistor. The waveforms in Figure 7 show an underdamped example with a 2 nF load and a 0 Ω external series gate resistor.

ADJUSTABLE DEAD TIME CONTROL

The ADuM4221/ADuM4221-1 include overlap protection such that the gate driver outputs (V_{OA} and V_{OB}) cannot simultaneously go high even if both inputs are high. Additionally, the ADuM4221/ADuM4221-1 also have a dead time control pin (DT) that can adjust the delay between the output high-side and low-side transitions by using a single resistor between the DT pin and ground (see Figure 34). The relationship between R_{DT} and the obtained dead time is shown in Figure 31.

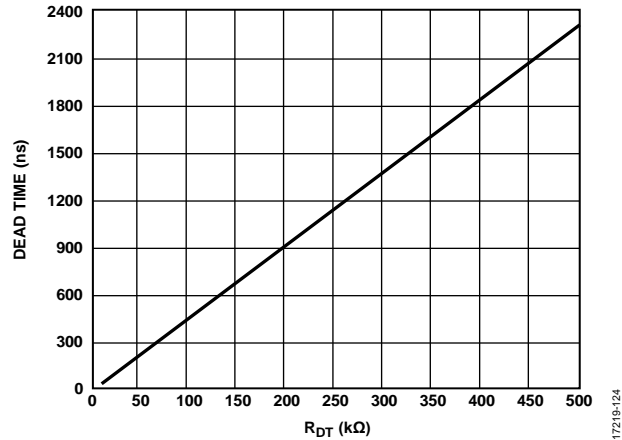
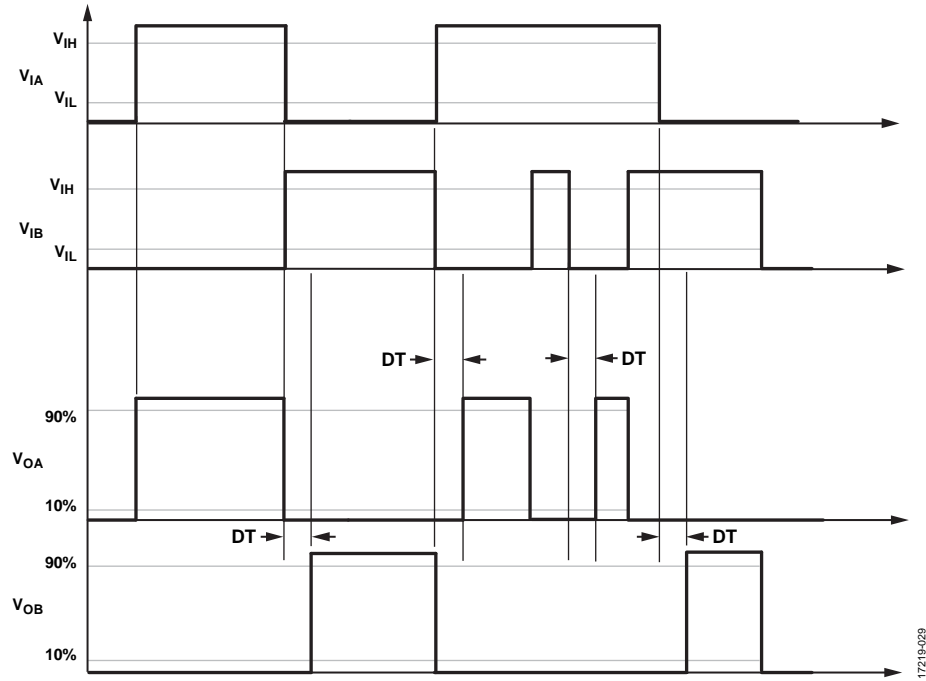


Figure 31. Dead Time vs. Dead Time Resistor

Use the following equation, to calculate the required amount of dead time:

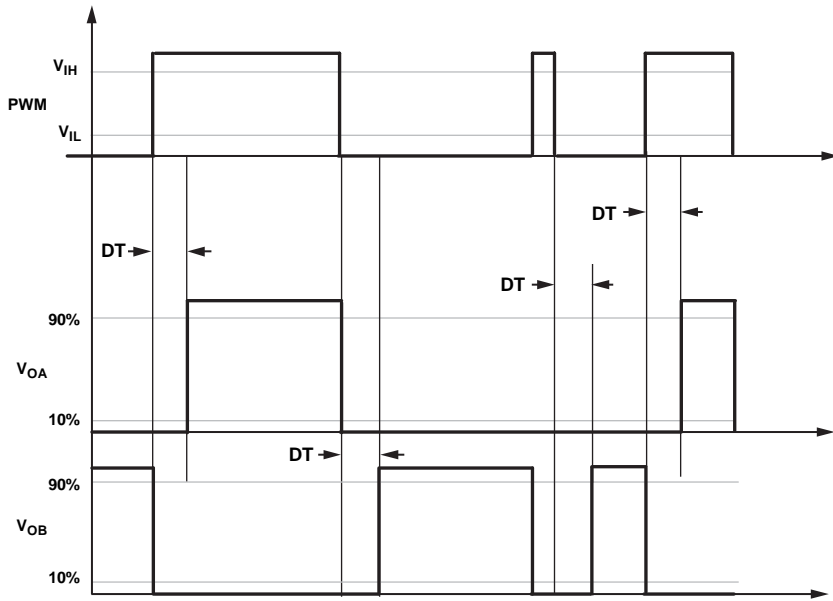
$$DT\ (ns) \approx 5 \times R_{DT}\ (k\Omega)$$

The V_{OA} and V_{OB} pins react to the V_{IA} and V_{IB} pins for the ADuM4221 only or the PWM pin for the ADuM4221-1 only depending on the dead time value set by the R_{DT} resistor. The DT pin controls the edge transitions between V_{OA} and V_{OB} . Dead time only affects the rising edge transition of the gate drive signal, and dead time operation is shown in Figure 32 and Figure 33.



17219-028

Figure 32. Dead Time Operation for Different Input Transitions for the ADuM4221



10450-302

Figure 33. Dead Time Operation for Different Input Transitions for ADuM4221-1

BOOTSTRAPPED, HALF BRIDGE OPERATION

The ADuM4221/ADuM4221-1 are well suited for operating two output gate signals referenced to separate grounds, as in the case for a half bridge configuration. Because isolated auxiliary supplies are often expensive, it is beneficial to reduce the amount of supplies.

One method to reduce power supplies is to use a bootstrapped configuration for the high-side supply of the ADuM4221 (see Figure 34). A similar setup can also be obtained for the ADuM4221-1. In this topology, the decoupling capacitor (C_A)

acts as the energy storage for the high-side supply and is filled whenever the low-side switch is closed, bringing GND_A to GND_B . During the C_A charging time, control the dv/dt of the V_{DDA} voltage to reduce the possibility of glitches on the output. To control the dv/dt of the V_{DDA} voltage, introduce a series resistance (R_{BOOT}) into the C_A charging path.

Note that in Figure 34, D_{BOOT} is the bootstrapped diode, C_{DD1} is the decoupling capacitor on the input side, and C_B is the decoupling capacitor for the driver low-side supply.

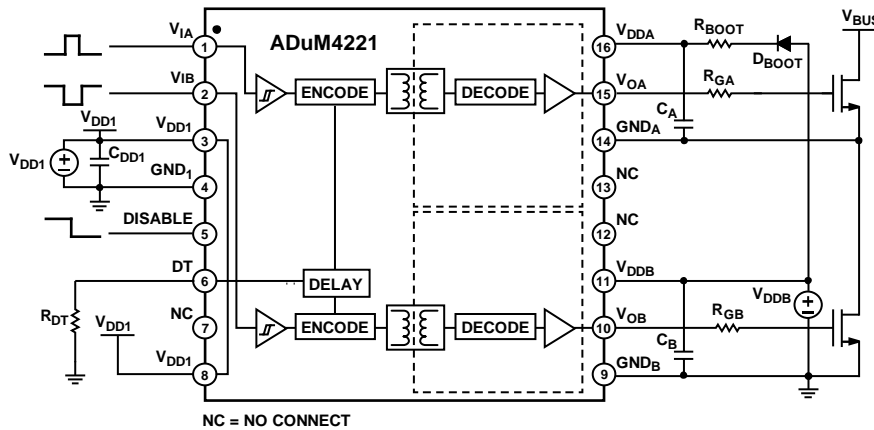


Figure 34. Bootstrapped, Half Bridge Operation Circuit for the ADuM4221

17Z19-024

POWER DISSIPATION

When driving a MOSFET or IGBT gate, the driver must dissipate power. This power is not insignificant and can lead to TSD if considerations are not made. The gate of an IGBT can be approximately simulated as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance of a given MOSFET or IGBT, C_{ISS} , and multiply this capacitance by a factor of 3 to 5 to arrive at a conservative estimate of the approximate load being driven. With this value, the estimated total power dissipation in the system due to the switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DD2} - GND_2)^2 \times f_{SW}$$

where:

$$C_{EST} = C_{ISS} \times 5.$$

f_{SW} is the switching frequency of the IGBT.

Alternately, use the gate charge as follows:

$$P_{DISS} = Q_G \times (V_{DD2} - GND_2) \times f_{SW}$$

where Q_G is the total gate charge of the devices being driven. This power dissipation is shared between the internal on resistances of the internal gate driver switches and the external gate resistances, R_{GON} and R_{GOFF} . The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4221/ADuM4221-1 devices.

$$\frac{P_{DISS_ADuM4221}}{P_{DISS_ADuM4221-1}} = P_{DISS} \times 0.5 \left(\frac{R_{DSON_P}}{R_{GON} + R_{DSON_P}} + 0.5 \left(\frac{R_{DSON_N}}{R_{GOFF} + R_{DSON_N}} \right) \right)$$

Take the power dissipation found inside the chip and multiply it by θ_{JA} to see the rise above ambient temperature that the ADuM4221/ADuM4221-1 experience, then multiply this value by two because there are two channels.

$$T_{ADuM4221}/T_{ADuM4221-1} = \theta_{JA} \times 2 \times P_{DISS_ADuM4221}/P_{DISS_ADuM4221-1} + T_A$$

For the devices to remain within specification, $T_{ADuM4221}/T_{ADuM4221-1}$ must not exceed 125°C. If $T_{ADuM4221}/T_{ADuM4221-1}$ exceeds the TSD rising edge, the devices enter TSD, and the output remains low until the TSD falling edge is crossed.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

The ADuM4221/ADuM4221-1 are resistant to external magnetic fields. The limitation on the ADuM4221/ADuM4221-1 magnetic field immunity is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which falsely sets or resets of the decoder can occur (see Figure 35 and Figure 36).

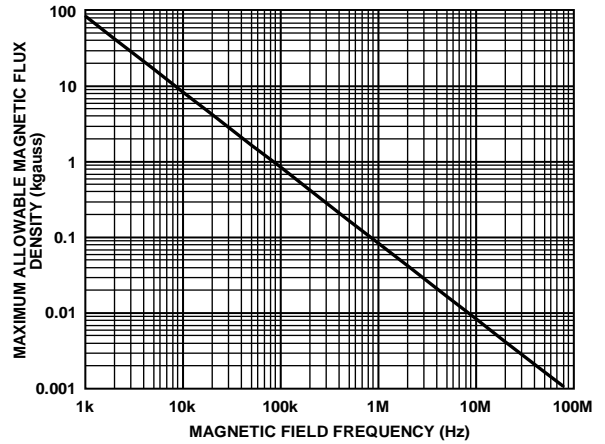


Figure 35. Maximum Allowable External Magnetic Flux Density

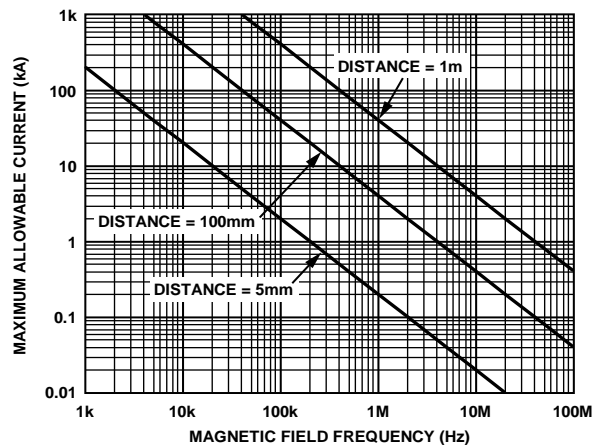


Figure 36. Maximum Allowable Current for Various Current to ADuM4221/ADuM4221-1 Spacings

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4221/ADuM4221-1.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values detailed in Table 9 summarize the peak voltage for 20 years of service life for a bipolar ac operating condition, and the maximum CSA and VDE approved working voltages. In many cases, the approved working voltage is higher than the 20 year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4221/ADuM4221-1 depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 37, Figure 38, and Figure 39 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst condition for iCoupler products and is the 20 year operating lifetime that Analog Devices recommends for the maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. Unipolar ac or dc voltage operation allows operation at higher working voltages while still achieving a 20 year service life. Any cross insulation voltage waveform that does not conform to Figure 38 or Figure 39 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 20 year lifetime voltage value listed in Table 9.

The voltage presented in Figure 38 is shown as sinusoidal for illustration purposes only. This voltage is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

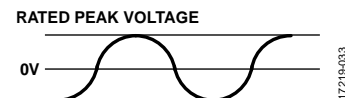


Figure 37. Bipolar AC Waveform

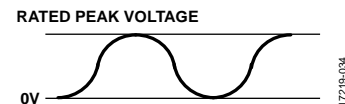


Figure 38. Unipolar AC Waveform

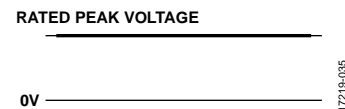
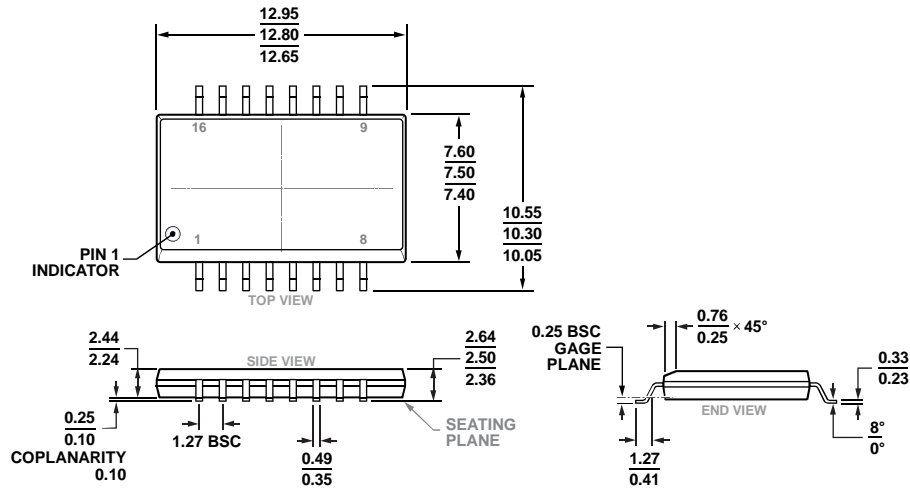


Figure 39. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC

Figure 40. 16-Lead Standard Small Outline Package with Increased Creepage [SOIC_IC] (RI-16-2)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Inputs	Minimum Output Voltage (V)	Adjustable Dead Time	Temperature Range	Package Description	Package Option	Ordering Quantity
ADuM4221ARIZ	V _{IA} , V _{IB}	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221ARIZ-RL	V _{IA} , V _{IB}	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC, 13" Tape and Reel	RI-16-2	1,000
ADuM4221BRIZ	V _{IA} , V _{IB}	7.5	Yes	-40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221BRIZ-RL	V _{IA} , V _{IB}	7.5	Yes	-40°C to +125°C	16-Lead SOIC_IC, 13" Tape and Reel	RI-16-2	1,000
ADuM4221CRIZ	V _{IA} , V _{IB}	11.6	Yes	-40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221CRIZ-RL	V _{IA} , V _{IB}	11.6	Yes	-40°C to +125°C	16-Lead SOIC_IC, 13" Tape and Reel	RI-16-2	1,000
ADuM4221-1ARIZ	PWM	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221-1ARIZ-RL	PWM	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC, 13" Tape and Reel	RI-16-2	1,000
ADuM4221-1BRIZ	PWM	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221-1BRIZ-RL	PWM	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC, 13" Tape and Reel	RI-16-2	1,000
ADuM4221-1CRIZ	PWM	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC	RI-16-2	1
ADuM4221-1CRIZ-RL	PWM	4.5	Yes	-40°C to +125°C	16-Lead SOIC_IC, 13" Tape and Reel	RI-16-2	1,000
EVAL-ADuM4221EBZ					Evaluation Board		
EVAL-ADuM4221-1EBZ					Evaluation Board		

¹ Z = RoHS Compliant Part.

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